

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,974,978 B1  
APPLICATION NO. : 09/262458  
DATED : December 13, 2005  
INVENTOR(S) : Possley

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

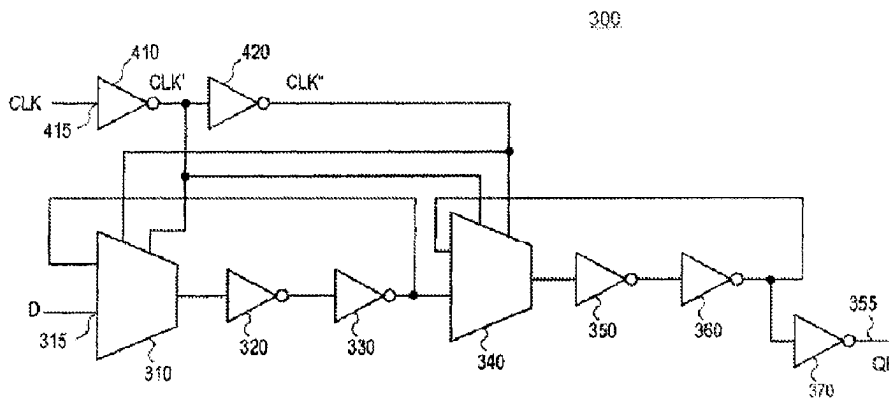
In the drawings:

Fig. 3

Reference numeral 320 appears twice in the drawing. The second appearance of "320" should read --370--. Insert reference numeral --300-- so it applies to the entire flip-flop.

Column 8

Lines 12-15, "... first one or more interconnects interconnecting exclusively first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors..." should read --... first one or more interconnects interconnecting exclusively first size transistors of one or more adjacent ones of the plurality of arrangements of first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors,...--.



**FIG. 3**

Signed and Sealed this

Twenty-seventh Day of October, 2009

*David J. Kappos*

David J. Kappos  
Director of the United States Patent and Trademark Office